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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,206	06/27/2003	Sang Moo Song	8733.847.00-US	5817

7590 09/08/2004

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EXAMINER	
NGUYEN, THANH NHAN P	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,206	SONG, SANG MOO	
	Examiner	Art Unit	
	(Nancy) Thanh-Nhan P Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 June 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The meaning of the claims is very unclear. Therefore, for the examination purposes, it would be interpreted as the thin film transistors (TFTs) coupled between an adjacent gate line, an adjacent data line, and the pixel electrode, wherein the length of a side of a pair of pixel electrodes adjacent a portion of a single data line are substantially equal, and wherein TFTs of consecutive ones of the plurality of liquid crystal cells arranged within vertical line are alternatively coupled to adjacent ones of the plurality of data lines.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al U.S. Patent Application Publication No. US 2002/0008792 A1.

Chung et al discloses a liquid crystal device (LCD) including a first substrate; a second substrate coupled to the first substrate; a plurality of scan lines and a plurality of data lines arranged over the first substrate, the scan lines intersecting the data lines to define pixel areas; thin film transistors (TFTs) over the first substrate adjacent intersections of the scan lines and data lines, and a liquid crystal layer interposed between the first and second substrates [see paragraph 0017 in Summary of the Invention]; at each pixel, parasitic capacitors, the capacitance of which are represented by Cdp1 and Cdp2, are created between each data line 13 and each pixel electrode 17 and between each pixel electrode 17 and each data line 13a, respectively, [see paragraph 0011 in Background of the Invention, and see figure 3]; an indium tin oxide (ITO) layer, for example, may be used as the pixel electrodes. In such a case, the lower left part of the ITO layers is removed to avoid the TFTs. In this example, the lower right part of the ITO layers are also removed as much as the lower left part of the ITO layers is removed to form the pixel electrode pattern that is bilaterally symmetric, [see paragraph 33 in Detailed Description, and see figure 6]. As shown in figure 6, the pixel electrode 47 is bilaterally symmetric. Therefore, the capacitance values Cdp1 and Cdp2 are substantially the same. In figure 6, because these parasitic capacitance values are substantially proportional to the length of the left most side and right most side, respectively, of the pixel electrode, Cdp1 and Cdp2 are symbolically represented by the length of the

sides of the pixel electrode 47. The LCD device of Chung et al, which has substantially bilaterally, symmetric pixel electrodes, has the benefit of improvement resolution characteristic in LCD.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, 6, 9-10, 12-14, 20-21, 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al in view of Kimura et al.

Referring to claims 2-3, from Chung et al disclosure above, Chung et al lacks a first horizontal line of liquid crystal cells having thin film transistors connected to preceding ones of adjacent data lines, and a second horizontal line of liquid crystal cells having thin film transistors connected to successive ones of adjacent data lines.

Also, referring to claim 6, Chung et al lacks within the first horizontal line, consecutive ones of the liquid crystal cells are charged with pixel signals having alternating, opposite polarities; within the second horizontal line, consecutive ones of the liquid crystal cells are charged with pixel signals having alternating, opposite polarities; and wherein within the first and second horizontal lines,

consecutive ones of the liquid crystal cells arranged within a vertical line, are charged with pixel signals having alternating, opposite polarities.

Kimura et al U.S. Patent No. 5,253,091 teaches the alternating of TFT connection to preceding ones of adjacent data lines, and the TFT connection to successive ones of adjacent data lines in every one horizontal line, and the use of dot inversion pixels for the benefit of reducing the screen flicker without increasing electric power consumption.

As Kimura et al shows in figure 4, gate drive circuit 1 is connected to n lines of the row signal conductors G1 to Gn, and supplies the gate signal Gn shown in Figure 5a. A first data drive circuit 2 is connected to the odd numbered signal conductors D1 to Dm-1, and provides the first data signal VDm shown in Figure 5b. A second data drive circuit 3 is connected to the even numbered signal conductors D2 to Dm (the last one not being shown), and provides the second data signal VDm+1 shown in figure 5c. As is apparent from figure 5, the polarity of the first data signal VDm, is opposite to the polarity of the second data signal VDm+1. Each gate electrode of the TFT's 4a, 4b, and 4c . . ., which drive respectively the pixels 5a, 5b, and 5c . . ., is connected to its respective row signal conductor. The drain electrodes of TFT's in each row as well as in each column are alternately connected to one of the odd numbered signal conductors D1 to Dm-1, and to one of the even numbered signal conductors D2 to Dm. Further, each source electrode of the TFT's 4a, 4b, 4c . . . is connected to a respective one of the pixels 5a, 5b, 5c . . . the gate signal VGn shown in figure 5a is applied sequentially to the row signal conductors G1 to Gn from the gate drive

circuit 1. All TFT's 4 connected to a row which is driven are turned on. Each row is activated sequentially. Synchronously with the application of the gate signal, during a frame cycle T, the first data signal VDm (figure 5b) from the first data drive circuit 2 and the second data signal VDm+1 (figure 5c) from second data drive circuit 3 are applied to the odd and even numbered column conductors, respectively. In this manner, the screen flicker is reduced as each pixel 5a, 5b, 5c . . . receives a data signal wherein the phase is shifted by 180 degrees between the adjacent pixels. This is true for adjacent pixels in successive rows, as well as for adjacent pixels in successive columns, [see column 3, lines 5-55, and figure 4].

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to arrange the TFT connection to preceding ones of adjacent data lines, and the TFT connection to successive ones of adjacent data lines in every one horizontal line alternatively besides the use of dot inversion pixels for the benefit of reducing the screen flicker without increasing electric power consumption.

Referring to claims 9-10, 12-13, 20-21, 26-27, Chung et al lacks the area/ length/ parasitic capacitance of a side of a pair of pixel electrodes adjacent a portion of a single data line are substantially equal; Chung et al lacks the TFT of consecutive ones of the plurality of liquid crystal cells arranged within a vertical line are alternately coupled to adjacent ones of the plurality of data lines.

Also, referring to claim 14, Chung et al lacks the consecutive ones of the liquid crystal cells arranged within a horizontal line are charged with data signals having opposite polarity.

Kimura et al teaches the flipping and alternating of the pixel electrodes so that the area/ length/ parasitic capacitance of a side of a pair of pixel electrodes adjacent a portion of a single data line are substantially equal, and the use of row inversion pixels for the benefit of reducing the flicker in the direction of the column, and less electrical power consumption.

Kimura et al shows in figure 7, the successive gate electrodes of the TFT's 4a, 4b, 4c . . . which each drive a successive, respective pixel 5a, 5b, 5c . . . in the direction of the row are alternately connected to one of the two adjacent row signal conductors. All drain electrodes of the TFT's 4a, 4b, 4c . . . in a given row are connected to the column signal conductors of only one of the data drive circuits. However, the drain electrodes of TFT's in successive rows are alternately connected to the column signal conductors of the first data drive circuit 2 and the column signal conductors of the second data drive circuit 3. In this case, the method of driving includes the application of the drive waveform in the manner shown in figure 5 to each pixel, to drive successive pixels in the direction of the row with the same polarity, and to drive successive pixels in the direction of the column alternately with positive and negative polarities; that is when one pixel is driven by a positive data signal an adjacent pixel in the direction of a column is driven by a negative data signal, [see column 4, lines 1-41, and figure 7].

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use the way of Kimura et al for flipping and alternating of the pixel electrodes so that the area/ length/ parasitic capacitance of a side of a pair of pixel electrodes adjacent a portion of a single data line are substantially equal, and to modify the use of row inversion pixels (of Kimura et al, to have screen flicker reduced in the direction of column, see column 4, lines 23-24) by using column inversion for the benefit of less electrical power consumption, and screen flicker reduced in the direction of row.

Claim 4 is rejected under 35 U.S.C. 103(a) over Chung et al in view of Kimura et al as applied above, and further in view of Suzuki U.S. Patent No. 5,436,747.

Chung et al lacks the first horizontal line and the second horizontal line are alternately arranged within the liquid crystal display panel, and wherein within a vertical line or liquid crystal cells, every two liquid crystal cells are liquid crystal cells from the first horizontal line.

Suzuki shows in figure 3 the alternating of TFT connection to preceding ones of adjacent data lines and the TFT connection to successive ones of adjacent data lines in every two horizontal lines for the benefit of reducing the screen flicker, and lowering the power consumption. Since the first and the second data drivers are not switched every two row conductors, as in figure 2, (instead of switching, the connection of each subpixel to each column conductor is changed), load on the data drivers decreases and the pixels can be driven by a circuit of relatively low power consumption. In other words, load on the data

drivers is reduced and the pixels may be driven by a low power consumption circuit because it is the connection of the column conductors which is changed to invert the polarities of the first and the second data signals every two row conductors. This is done instead of using high speed, high amplitude electric switching, [see column 4, lines 63-68; column 5, lines 1-8; and figure 2, 3].

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to arrange alternatively every two horizontal lines, and wherein within a vertical line of liquid crystal cells, every two liquid crystal cells are from the first horizontal line for the benefit of having reduced flicker and low power consumption.

Referring to claim 11, also missing from the first reference, by Chung at el, is the thin film transistors of every two consecutively arranged ones of the plurality of liquid crystal cells arranged within a vertical line are alternately coupled to adjacent ones of the plurality of data lines. This is the case of flipping and alternating of the pixel electrodes of every two horizontal lines so that the thin film transistors of every two consecutively arranged ones of the plurality of liquid crystal cells arranged within a vertical line are alternately coupled to adjacent ones of the plurality of data lines. Since Kimura et al teaches about flipping of the pixel electrodes of every one horizontal line, and Suzuki teaches about alternating of the pixel electrodes of every two horizontal lines, it would have been obvious to a person of ordinary skill in the art to modify to have flipping and alternating of the pixel electrodes of every two horizontal lines for the benefit of having reduced flicker and low power consumption.

Claims 15-19, 22-25 are rejected because the parasitic capacitance values are substantially proportional to the length of the side of the pixel electrodes; Cdp1 and Cdp2 are symbolically represented by the length of the sides of the pixel electrodes, [see paragraph 41 in First Embodiment of Chung et al]. The cut-out portion of the electrode is opposite with the other portion of the electrode, where the TFT's drain electrode connected to. So, it really does not matter at what portion the TFT is placed, the cut-out portion, which may be in the upper, lower, or middle part, is always opposite to the TFT position for the benefit of having the same side length at left most side and at right most side in order to reduce or nearly eliminate the resolution degradation of the LCD. It has been determined that the rearrangement of parts is within the ordinary level of skill, [see MPEP 2144.04 VI (C) Rearrangement of Parts]. Further, having the same side length at left most side and at right most side in order to reduce the resolution degradation of the LCD, the cut-out portion in the upper, lower, or middle part might also want to avoid the spacers or the color filters in the LCD. Therefore, it would have been obvious to a person of ordinary skill in the art to place the cut-out portion at the upper or in the middle of the side length of the electrode pixels since the rearrangement of the parts is within the ordinary skill level, and for the benefit of reducing or nearly eliminating the resolution degradation of the LCD.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chung et al U.S. Patent Application Publication No. US 2002/0008792 A1 disclose the substantially bilaterally, symmetric pixel electrodes for the benefit of improvement resolution characteristic in LCD.

Kimura et al U.S. Patent No. 5,253,091 disclose the use of dot inversion, and the alternating of every one horizontal line of TFT connection to preceding ones of adjacent data lines and the TFT connection to successive ones of adjacent data lines for the benefit of reducing the screen flicker. Kimura also discloses the flipping of the pixel electrodes so that the area/ length/ parasitic capacitance of a side of a pair of pixel electrodes adjacent a portion of a single data line are substantially equal, and the use of row inversion pixels for the benefit of using less electrical power consumption, and reducing the flicker in the direction of the column.

Suzuki U.S. Patent No. 5,436,747 discloses the alternating of TFT connection to preceding ones of adjacent data lines and the TFT connection to successive ones of adjacent data lines in every two horizontal lines for the benefit of reducing the screen flicker, and lowering the power consumption.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P Nguyen whose

telephone number is 571-272-1673. The examiner can normally be reached on M-F/9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

(Nancy) Thanh-Nhan P Nguyen
Examiner
Art Unit 2871

TN

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